Standard Power MOSFETs

IRFF110, IRFF111, IRFF112, IRFF113

File Number **1562**

Power MOS Field-Effect Transistors

N-Channel Enhancement-Mode Power Field-Effect Transistors

3.0A and 3.5A, 60V-100V

r_{DS}(on) = 0.6 Ω and 0.8 Ω

Features:
- SOA is power-dissipation limited
- Nanosecond switching speeds
- Linear transfer characteristics
- High input impedance
- Majority carrier device

The IRFF110, IRFF111, IRFF112 and IRFF113 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.
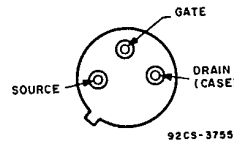
The IRFF-types are supplied in the JEDEC TO-205AF (LOW-PROFILE TO-39) metal package.

N-CHANNEL ENHANCEMENT MODE

92CS-33741
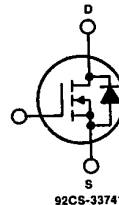
TERMINAL DIAGRAM

TERMINAL DESIGNATION

92CS-37555

JEDEC TO-205AF

Absolute Maximum Ratings

	Parameter	IRFF110	IRFF111	IRFF112	IRFF113	Units
V_{DS}	Drain - Source Voltage ①	100	60	100	60	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 20 KΩ) ①	100	60	100	60	V
I_D @ T_C = 25°C	Continuous Drain Current	3.5	3.5	3.0	3.0	A
I_{DM}	Pulsed Drain Current ③	14	14	12	12	A
V_{GS}	Gate - Source Voltage	± 20				V
P_D @ T_C = 25°C	Max. Power Dissipation	15 (See Fig. 14)				W
	Linear Derating Factor	0.12 (See Fig. 14)				W/°C
I_{LM}	Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH				A
		14	14	12	12	
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

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Electrical Characteristics @T$_C$ = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions	
BV$_{DSS}$	Drain - Source Breakdown Voltage	IRFF110 IRFF112	100	–	–	V	$V_{GS} = 0V$ $I_D = 250\mu A$	
		IRFF111 IRFF113	60	–	–	V		
V$_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4.0	V	$V_{DS} = V_{GS}, I_D = 250\mu A$	
I$_{GSS}$	Gate-Source Leakage Forward	ALL	–	–	100	nA	$V_{GS} = 20V$	
I$_{GSS}$	Gate-Source Leakage Reverse	ALL	–	–	–100	nA	$V_{GS} = -20V$	
I$_{DSS}$	Zero Gate Voltage Drain Current	ALL	–	–	250	μA	$V_{DS} =$ Max. Rating, $V_{GS} = 0V$	
			–	–	1000	μA	$V_{DS} =$ Max. Rating x 0.8, $V_{GS} = 0V, T_C = 125°C$	
I$_{D(on)}$	On-State Drain Current ②	IRFF110 IRFF111	3.5	–	–	A	$V_{DS} \rangle I_{D(on)} \times R_{DS(on)}$ max., $V_{GS} = 10V$	
		IRFF112 IRFF113	3.0	–	–	A		
R$_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRFF110 IRFF111	–	0.5	0.6	Ω	$V_{GS} = 10V, I_D = 1.5A$	
		IRFF112 IRFF113	–	0.6	0.8	Ω		
g$_{fs}$	Forward Transconductance ②	ALL	1.0	1.5	–	S (℧)	$V_{DS} \rangle I_{D(on)} \times R_{DS(on)}$ max., $I_D = 1.5A$	
C$_{iss}$	Input Capacitance	ALL	–	135	200	pF	$V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz$ See Fig. 10	
C$_{oss}$	Output Capacitance	ALL	–	80	100	pF		
C$_{rss}$	Reverse Transfer Capacitance	ALL	–	20	25	pF		
t$_{d(on)}$	Turn-On Delay Time	ALL	–	10	20	ns	$V_{DD} = 0.5 BV_{DSS}, I_D = 1.5A, Z_0 = 50\Omega$ See Fig. 17, (MOSFET switching times are essentially independent of operating temperature.)	
t$_r$	Rise Time	ALL	–	15	25	ns		
t$_{d(off)}$	Turn-Off Delay Time	ALL	–	15	25	ns		
t$_f$	Fall Time	ALL	–	10	20	ns		
Q$_g$	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	–	5.0	7.5	nC	$V_{GS} = 10V, I_D = 8.0A, V_{DS} = 0.8$ Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)	
Q$_{gs}$	Gate-Source Charge	ALL	–	2.0	–	nC		
Q$_{gd}$	Gate-Drain ("Miller") Charge	ALL	–	3.0	–	nC		
L$_D$	Internal Drain Inductance	ALL	–	5.0	–	nH	Measured from the drain lead, 5 mm (0.2 in.) from header to center of die.	Modified MOSFET symbol showing the internal device inductances.
L$_S$	Internal Source Inductance	ALL	–	15	–	nH	Measured from the source lead, 5mm (0.2 in.) from header to source bonding pad.	
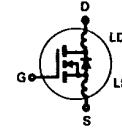
Thermal Resistance

R$_{thJC}$	Junction-to-Case	ALL	–	–	8.33	°C/W	
R$_{thJA}$	Junction-to-Ambient	ALL	–	–	175	°C/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

I$_S$	Continuous Source Current (Body Diode)	IRFF110 IRFF111	–	–	3.5	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRFF112 IRFF113	–	–	3.0	A	
I$_{SM}$	Pulse Source Current (Body Diode) ③	IRFF110 IRFF111	–	–	14	A	
		IRFF112 IRFF113	–	–	12	A	
V$_{SD}$	Diode Forward Voltage ②	IRFF110 IRFF111	–	–	2.5	V	$T_C = 25°C, I_S = 3.5A, V_{GS} = 0V$
		IRFF112 IRFF113	–	–	2.0	V	$T_C = 25°C, I_S = 3.0A, V_{GS} = 0V$
t$_{rr}$	Reverse Recovery Time	ALL	–	200	–	ns	$T_J = 150°C, I_F = 3.5A, dI_F/dt = 100A/\mu s$
Q$_{RR}$	Reverse Recovered Charge	ALL	–	1.0	–	μC	$T_J = 150°C, I_F = 3.5A, dI_F/dt = 100A/\mu s$
t$_{on}$	Forward Turn-on Time	ALL					Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.

① T$_J$ = 25°C to 150°C. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

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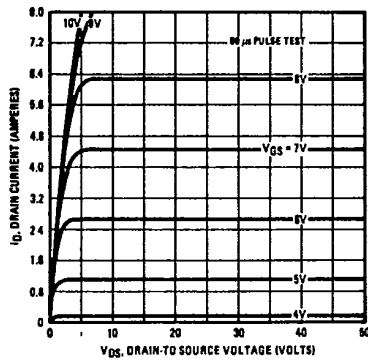## IRFF110, IRFF111, IRFF112, IRFF113

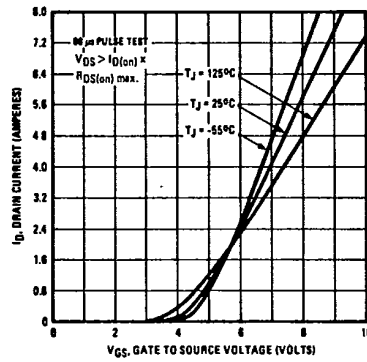Fig. 1 — Typical Output Characteristics

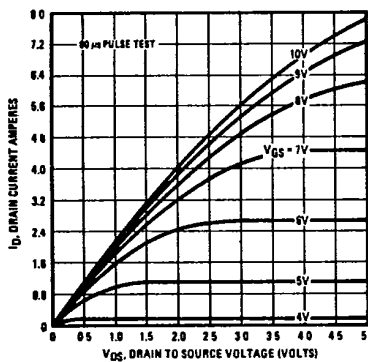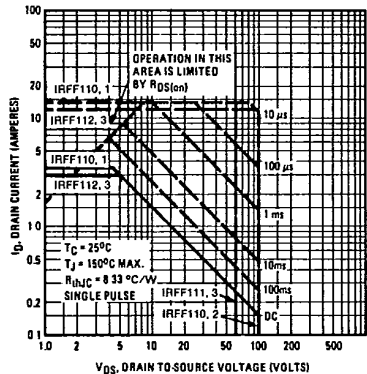Fig. 2 — Typical Transfer Characteristics

Fig. 3 — Typical Saturation Characteristics
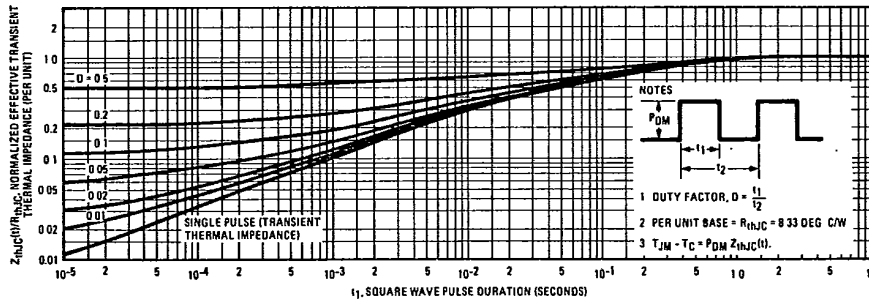

Fig. 4 — Maximum Safe Operating Area

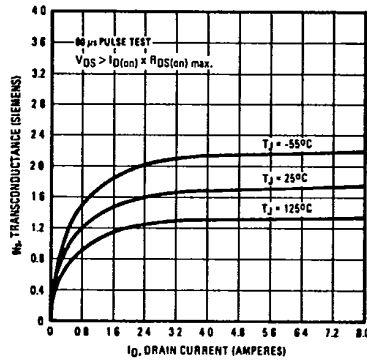Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

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Fig. 6 — Typical Transconductance Vs. Drain Current
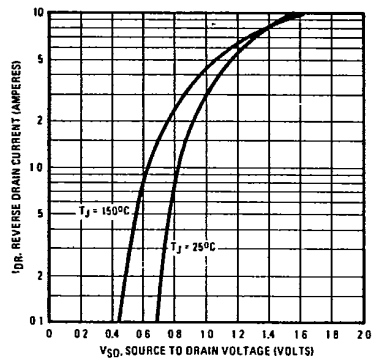
Fig. 7 — Typical Source-Drain Diode Forward Voltage
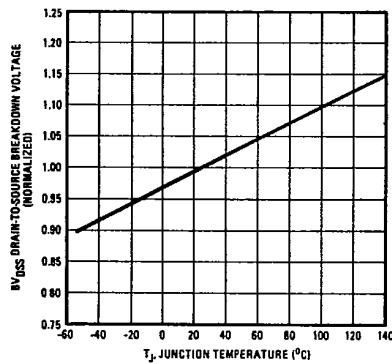
Fig. 8 — Breakdown Voltage Vs. Temperature
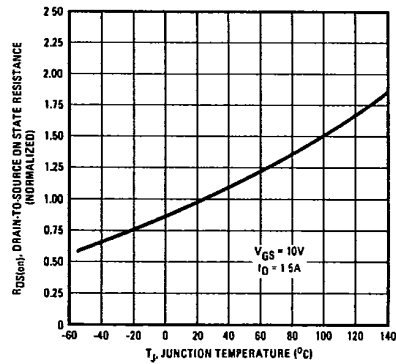
Fig. 9 — Normalized On-Resistance Vs. Temperature
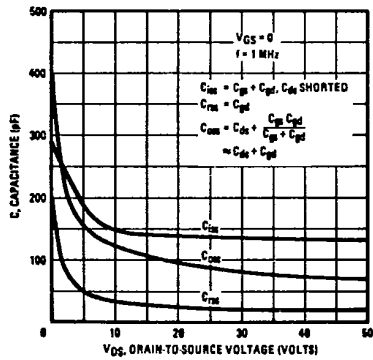
Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage
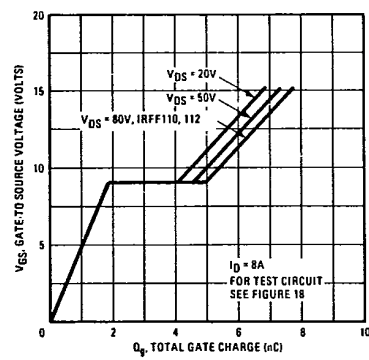
Fig. 11 — Typical Gate Charge Vs. Gate-to-Source Voltage

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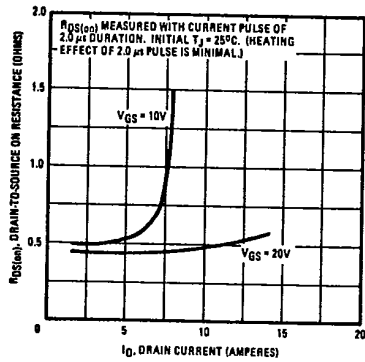
Fig. 12 — Typical On-Resistance Vs. Drain Current
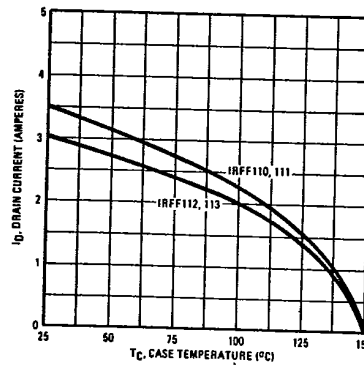
Fig. 13 — Maximum Drain Current Vs. Case Temperature
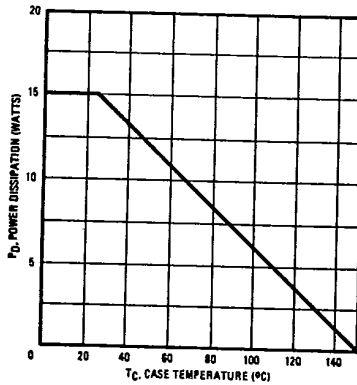
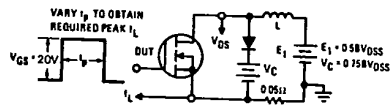Fig. 14 — Power Vs. Temperature Derating Curve
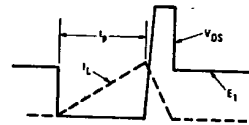

Fig. 15 — Clamped Inductive Test Circuit
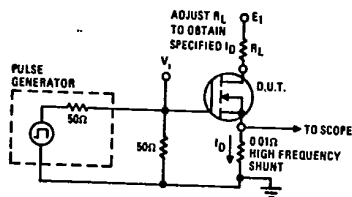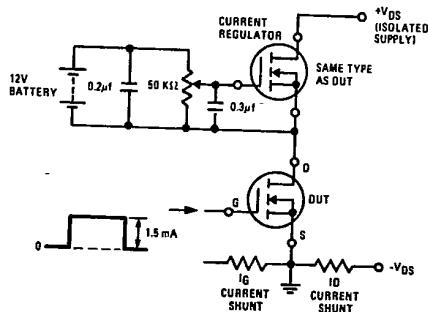

Fig. 16 — Clamped Inductive Waveforms

Fig. 17 — Switching Time Test Circuit

Fig. 18 — Gate Charge Test Circuit